What is claimed is:

1. A non-volatile semiconductor memory device, comprising:

a memory cell array having electrically erasable and programmable non-volatile memory cells, a part of said memory cell array being defined as a initial set-up data region for storing a plurality of initial set-up data that define memory operation conditions;

a plurality of data latch circuits for holding the respective initial set-up data read out from said initial set-up data region;

a controller for controlling data program and erase operations for said memory cell array; and

a clock generator for generating a clock signal that is used to define an operation timing of said controller, wherein

said controller is configured to perform such an initial set-up operation that sequentially reads out said plurality of initial set-up data stored in said initial set-up data region and transfers them to the respective data latch circuits on receipt of power-on or a command input, said initial set-up operation being so performed as to read out a clock cycle adjustment data within said plurality of initial set-up data stored in said initial set-up data region in the beginning, thereby adjusting a clock cycle of said clock signal output from said clock generator by use of said clock cycle adjustment data, and

then reads out the remaining initial set-up data by use of the adjusted clock signal.

2. The memory device according to claim 1, further comprising:

a power-on detecting circuit for detecting power-on to activate said controller to perform said initial set-up operation.

3. The memory device according to claim 1, wherein said clock generator comprises:

a ring oscillator; and

a delay circuit disposed in said ring oscillator, a delay time of which being defined by said clock cycle adjustment data.

4. The memory device according to claim 3, wherein said delay circuit comprises a CR time constant circuit having a resister and a capacitor, at least one of said resister and capacitor being variably controlled in response to said clock cycle adjustment data.

5. The memory device according to claim 1, further comprising:

a boost circuit for boosting a power supply voltage in response to power-on to supply a boosted voltage to a power supply node of said clock generator.

6. The memory device according to claim 1, wherein said controller has a test mode so programmed as to check said initial set-up data stored in said initial set-up data region of said memory cell array on receipt of a

command input from an external terminal.

7. The memory device according to claim 1, wherein said controller has a test mode so programmed as to rewrite said initial set-up data stored in said initial set-up data region of said memory cell array on receipt of a command input from an external terminal.

8. The memory device according to claim 1, wherein said controller has a test mode so programmed as to check said initial set-up data stored in said data latch circuits on receipt of a command input from an external terminal.

9. The memory device according to claim 1, wherein said controller has a test mode so programmed as to rewrite said initial set-up data stored in said data latch circuits on receipt of a command input from an external terminal.

10. The memory device according to claim 1, wherein said memory cell array has a plurality of NAND cell units each of which has a plurality of serially connected memory cells and a select transistor through which said serially connected memory cells are connected to a bit line, said serially connected memory cells being driven by different word lines from each other.

11. A non-volatile semiconductor memory device, comprising:

a memory cell array having electrically erasable and programmable non-volatile memory cells, a part of said

memory cell array being defined as a initial set-up data region for storing a plurality of initial set-up data that define memory operation conditions;

data latch circuits for holding said initial set-up data read out from said initial set-up data region;

a controller for controlling data program and erase operations for said memory cell array;

a clock generator for generating a clock signal that is used to define an operation timing of said controller;

a first boost circuit for outputting a boosted voltage necessary for data read, program and erase of said memory cell array; and

a second boost circuit for boosting a power supply voltage in response to power-on to supply a boosted voltage to a power supply node of said clock generator.

12. The memory device according to claim 11, wherein said controller is configured to perform such an initial set-up operation that sequentially reads out said plurality of initial set-up data stored in said initial set-up data region and transfers them to the respective data latch circuits on receipt of power-on or a command input, said initial set-up operation being so performed as to read out a clock cycle adjustment data within said plurality of initial set-up data stored in said initial set-up data region in the beginning, thereby adjusting a clock cycle of said clock signal output from said clock generator by use of said clock cycle adjustment data, and

then reads out the remaining initial set-up data by use of the adjusted clock signal.

13. The memory device according to claim 11, further comprising:

a power-on detecting circuit for detecting power-on to activate said controller to perform said initial set-up operation.

14. The memory device according to claim 11, wherein said clock generator comprises:

a ring oscillator; and

a delay circuit disposed in said ring oscillator, a delay time of which being defined by said clock cycle adjustment data.

15. The memory device according to claim 14, wherein said delay circuit comprises a CR time constant circuit having a resister and a capacitor, at least one of said resister and capacitor being variably controlled in response to said clock cycle adjustment data.

16. The memory device according to claim 11, wherein said controller has a test mode so programmed as to check said initial set-up data stored in said initial set-up data region of said memory cell array on receipt of a command input from an external terminal.

17. The memory device according to claim 11, wherein said controller has a test mode so programmed as to rewrite said initial set-up data stored in said initial set-up data region of said memory cell array on receipt of

a command input from an external terminal.

18. The memory device according to claim 11, wherein said controller has a test mode so programmed as to check said initial set-up data stored in said data latch circuits on receipt of a command input from an external terminal.

19. The memory device according to claim 11, wherein said controller has a test mode so programmed as to rewrite said initial set-up data stored in said data latch circuits on receipt of a command input from an external terminal.

20. The memory device according to claim 11, wherein said memory cell array has a plurality of NAND cell units each of which has a plurality of serially connected memory cells and a select transistor through which said serially connected memory cells are connected to a bit line, said serially connected memory cells being driven by different word lines from each other.